(19) Europäisches Patentamt
European Patent Office
Office européen des brev ts

(11) Publication number: **0 333 942**
A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **88302479.6**

(51) Int. Cl.4: **H04J 3/06**

(22) Date of filing: **22.03.88**

(43) Date of publication of application:
27.09.89 Bulletin 89/39

(84) Designated Contracting States:
AT BE CH DE ES FR GB GR IT LI LU NL SE

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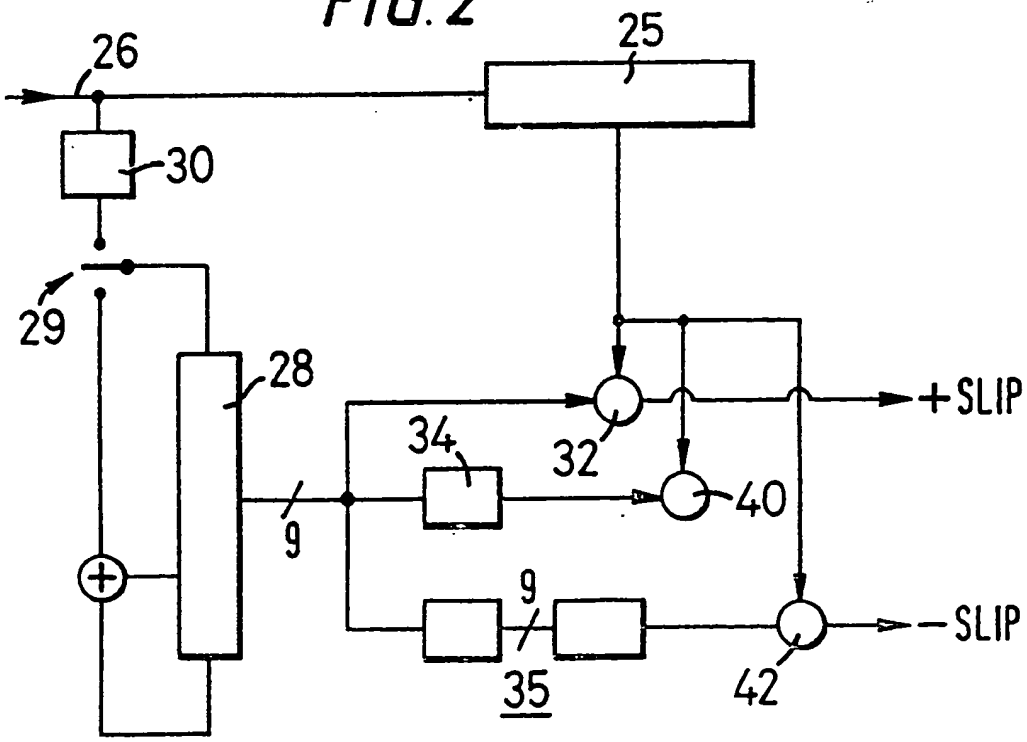
(54) Monitoring of digital transmission systems.

(57) An arrangement for monitoring slip in a digital transmission system. A PRBS sequence is transmitted in one channel or timeslot of the system. At a receiving station a characteristic group of N bits of the received sequence is assembled. The assembled group is compared with locally formed groups of N bits which would be expected to occur if a slip has occurred.

FIG. 2



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Monitoring of Digital Transmission Systems

This invention relates to digital transmission systems and in particular relates to the monitoring of such systems.

In digital transmission systems, digital data is transmitted typically between telephone exchanges. At the source end, data is clocked out onto a telephone line under the control of a clock associated with the source exchange. At the receive end, data is fed into an elastic store under the control of clock signals derived from the transmitted data stream. Data is then fed out from the elastic store under the control of a local clock in the source exchange. The elastic store is provided so that it can accommodate any phase difference between the clocks of the two exchanges. However, problems arise when there are differences in the frequencies of the two clocks. If there are such differences then the elastic store will either fill up or become empty depending upon the direction of the difference.

An elastic store in a transmission system operating typrically at 1.544 Mbit/sec, has a capacity of 192 bits which is the number of bits in a frame. The elastic store can be conceptualised as a circular buffer, which is accessed by two pointers, one of which controls reading into the store and the other of which controls reading out from the store. Thus, data is entered at a location corresponding to one pointer, which is then advanced to the next location, whilst data is extracted under the control of the other pointer, which is then advanced in a similar manner. Initially the pointers are 96 bits apart, i.e. one half frame. The buffer becomes full or empty when the pointers meet, which can occur if the frequencies of the clocks referred to above are not the same. When the pointers cross, the phenomenon known as a controlled slip occurs. If the pointer associated with the incoming data overtakes the pointer associated with the clocking out of data, a whole frame of data is deleted. This is known as negative slip. Conversely if the pointer associated with clocking out of the data overtakes the pointer associated with clocking in of data, then a whole frame of data is duplicated. This is known as positive slip. In either case it is important that such phenomena can be sensed and identified.

There have been various attempts at measurement of slip. A fairly basic technique is to measure the frequency difference between the two clock signals and from this to derive the number of slips per unit time. This method, however, does not indicate the exact instant at which a slip occurs.

Slips can also be measured by sensing the sequencing of data. When a slip occurs, data in each time slot of a frame is deleted or duplicated depending on whether the slip is negative or positive. Because of this, slip measurements need not be made on data within a whole frame, but can be made using data within one time slot of that frame. Thus it is possible to take a single channel out of service and to use that channel to sense slip.

In order to sense slip using this general technique, it is necessary to stimulate in a time slot a data pattern which has a characteristic that its sequence is known. A bit stream that has such a characteristic is a pseudo random binary sequence (PRBS). A PRBS generates a determined bit stream. If a received bit stream is shown to have jumped forward by n bits (assuming an n bit time slot), then a negative slip has occurred. Conversely, if it has jumped backward by n bits then a positive slip has occurred. PRBS streams are used in digital transmission systems to detect errors. It has also been proposed to use such streams to sense slip, although existing methods, which compare the n of bits received in a time slot with the n bits expected if a slip has occurred, can give false slip measurements. This is because the number of bits n used in the comparison is less than the number of bits N which characterise a PRBS. A group of n bits can be repeated in a PRBS and give a false indication of a slip. An object of the present invention is to provide a technique for monitoring slip in digital transmission arrangements, which does not have such problems.

According to the present invention there is provided apparatus for monitoring slip in a digital transmission system, in which digital data is received in a store and re-aligned to a local clock, said apparatus comprising means for receiving said data from said store and for accumulating a characteristic group of N successive bits of a PRBS sequence transmitted with said data, means for forming groups of N bits of a PRBS sequence which would be expected in the event of a slip, and means for comparing the accumulated N bits with said groups of predicted bits.

The group of N bits may be accumulated from N-n PRBS bits of a first slot (n bits per time slot) and n PRBS bits of the next succeeding time slot. The accumulation and generation of expected values may be carried out by a processor. The expected PRBS bits may be generated using a look-up table technique.

The invention will be described now, by way of example only, with particular reference to the accompanying drawings. In the drawings:

Figure 1 is a block schematic diagram showing a digital transmission arrangement and an apparatus for monitoring slip in accordance with the present invention;

Figure 2 illustrates one implementation of slip monitoring apparatus, and Figure 3 shows how a processor based embodiment may generate PRBS's.

A digital transmission system typically comprises a source exchange 10, which is coupled to a receiving exchange 11 by a telephone lin 12. Data is clocked out from the source exchange 10 onto the telephone line 12 under the control of a clock at the source end. At the receiv exchange, data is fed into an elastic store 14 via a circuit 15 which extracts clock signals from the incoming data to gen rate write control signals for controlling the writing of data into the store 14. The data is then fed out from the elastic store 14 under the control of clock signals generated from a local clock 16 in the receiving exchange.

Apparatus for measuring slip in the transmission arrangement is shown generally at 20. It can be implemented using a processor which has the capability of generating PRBS sequences.

Digitally encoded data is typically generated and transmitted in frames, each of which comprises a number of time slots or channels. In the present technique, one of these time slots is taken out of service and used to transmit a PRBS sequence from the source exchange 10. Such a facility is usually available in a transmission arrangement, since it is known to use PRBS'S for the detection of errors. The apparatus 20 is designed to monitor the received PRBS sequence by forming from that incoming sequence what is called a PRBS state vector which is a group of N bits which characterises that incoming PRBS. The apparatus compares that state vector with locally generated values of such a state vector, which would be expected to occur a slip had occurred. On the basis of this comparison the apparatus can produce an appropriate indication when a slip is indicated.

PRBS'S comprises 2^N-1 bits and are uniquely characterised by a group of N bits. By looking at any group of N bits, it is possible to identify the position of that group of bits in the PRBS sequence.

Typically PRBS'S used in digital data transmission systems are either 2^9-1, i.e. 511, or 2^{11}-1, i.e. 2047 bits in length. Such sequences are uniquely characterised either by 9 or 11 bits. Only by looking at the characteristic number of bits can the sequence be unambiguously characterised. In digital data transmission systems there are typically 8 bits per channel. Thus, by looking at the 8 bits of a channel it is not possible to uniquely characterise the PRBS sequence. This is because sequences of fewer bits than the 9 or 11 will occur multiple times within the PRBS sequence. Furthermore, PRBS's will generate 8 bit sequences that run consecutively. Thus, slip cannot be sensed simply by comparing an 8 bit time slot of a frame with predicted values for the 8 bits on either side of that time slot.

The apparatus 20 overcomes this problem by tracking the last 9 bits (N = 9) of the received PRBS fed out from the elastic store 15 and compares those 9 bits with the 9 bits that would be expected if slip has occurred. Thus the apparatus 20 has to generate: (1) the previous 9 PRBS bits to check for negative slips, (2) the next 9 PRBS bits to check for positive slips and (3) in addition the current 8 bits for error counting.

The apparatus 20 compares the last 9 bits of the received PRBS and if it finds identity with either of the predicted values, generates an output indicating a negative or a positive slip. Appropriate action can then be taken in response to such a slip measurement.

Figure 2 shows schematically one implementation of the apparatus 20. The apparatus comprises a shift register 25 for storing the 9 bit PRBS state vector formed from the incoming PRBS fed out from the elastic store onto line 26. The apparatus also includes a PRBS generator 28 which is coupled to the line 26 by a switch 29 and a delay element 30. The output from the generator 28 is connected to a bitwise comparator 32, which is arranged to compare that output with the contents of the register 25, a circuit 34 which receives the current PRBS state and predicts its value after 8 clock periods and a circuit 35 which receives the current PRBS state and predicts its value after 16 clock periods (2 frames). The output of the circuit 34 is applied to a comparator 40 which is arranged to compare that output with the contents of the shift register 25 and the output of the circuit 35 is applied to a bitwise comparator 42 which is arranged to compare that output with the contents of the shift register 25.

In use the switch 29 is initially set to its upper position, as seen in Figure 2. This enables the generator 28 to be trained or aligned to the incoming bit stream. It should be noted that it is trained so that it is in the state that the bit stream was in n clock periods (where n is usually 8) previously, i.e. it is phase shifted with respect to the bit stream. The switch 29 is then set to its lower position so that the generator 28 is set to its feedback mode. Incoming bits are collected in the shift register 25. A frame is known to have been duplicated (positive slip) if the contents of the shift register 25 and the contents of the PRBS register are equal. This is sensed by the comparator 32 which produces an output indicative of positive slip.

To determine if a frame has been deleted (negative slip) the circuit 35 calculates a PRBS state vector as if 2n bits (two frames) had arrived. The comparator 42 produces an output in the event of negative slip.

The apparatus 20 can alternatively b a processor with the capability of generating PRBS's using a look-up table technique. The processor operates to form a 9 bit PRBS state vector from the incoming

stream, computes state vectors which would be expected if positive or negative slip had occurred and makes a comparison of the state v ctor with the expected values to sense if slip has occurred.

The algorithm which is used to control the operation of the processor, is as follows. The algorithm assumes:-

there are 8 PRBS bits per time slot; i.e. 64 kbit/s, the PRBS is 511, (2^9-1).
[adjustments are possible for 56 kbit/s and an 11 stage PRBS]. Algorithm is as follows:-

```
read in 8 bits; save the youngest bit.
read in 8 bits; merge with the saved bit to form the
"PRBS_state_vector",
        save the youngest bit.
loop_point:

read in 8 bits; form a 9-bit state vector "This_PRBS_
state".
            if This_PRBS_state -- PRBS_state_vector then
               a positive slip has occurred.
          goto loop_point
          endif
            PRBS_state_vector :- next(PRBS_state_vector)
        count bit wise differences between the received 8
        bit word
            and the least significant 8 bits of the PRBS_
            state_vector.
        This count is the error count.


           if This_PRBS_state -- next(PRBS_state_vector)
             a negative slip has occurred
        PRBS_state_vector :- This_PRBS_state.
        goto loop_point
        endif
```

In this algorithm next(state) represents a function/macro which given a PRBS state predicts what the PRBS state will be after 8 clock periods. The way in which PRBS'S can be generated by a processor is described later.

It will be noted that the above algorithm includes an error detecting step. It should be noted that the presence of errors can affect the slip measurement. The presence of error can change any pattern to any other pattern and therefore can affect the algorithm used to control the operation of the processor. In the present arrangement when a slip is recognised it does not require gaining of a new PRBS alignm nt. The unique 9 bits that synchronise the PRBS has already been determined for the slip measurement. Therefore when a slip has been detected the algorithm immediately takes up the new alignment. If a slip had been simulated by errors in the bit stream, this algorithm immediately recognises this and reports a slip of the opposite direction. Since the frequencies of the two clocks are never that different, genuine slips will be infrequent. Therefore if two slips are reported consecutively it is apparent that a slip has been seen as a result of line errors. In this case a slip reading can be suppressed if required.

The following example will illustrate how this algorithm can work for an arrangement in which there are 8 data bits per byte and in which a 9 stage PRBS is used. The example shows 4 successive groups of 8 bits where there is no slip where there is positive slip and where there is negative slip.

```
        -------> time ---------------------->
        oldest/first received          youngest/last
                                       received
          byte 1    byte 2    byte 3    byte 4
0 slip    AAAAAAAA  BBBBBBBB  CCCCCCCC  DDDDDDDD
+ slip    aaaaaaaa  bbbbbbbb  bbbbbbbb  cccccccc
- slip    aaaaaaaa  bbbbbbbb  dddddddd  eeeeeeee
                               ^         ^
                               T0        T1
```

at T0 alignment to the PRBS is accomplished using the last two received bytes; the PRBS state is bbbbbbbba; NB whereas time in the bit stream (above) runs from left to right, it is convention to for PRBS state to show the least-significant (newest) bit on the right and therefore in a register representation time runs from right to left.

Therefore at T0, two bytes have been received and processed; the PRBS state will have been determined from the last n (8) bits from the latest frame and the previous N-n (1) bits to make 9 bits in all; i.e. BBBBBBBA.

At T1 the next two bytes will have been received. The current PRBS state is determined using the received PRBS state and predicting it's value after 16 bits.

If it is equal to the state received then no slip has occurred. Besides predicting the state after 16 clock periods, the state is predicted for both 8 and 24 clock periods hence.

If the received vector equals either then a slip (of the appropriate kind) has occurred; and as a slip is known to have occurred the local PRBS state can be updated immediately without another training sequence (of the kind noted at time T0).

Figure 3 shows how the processor can generate PRBS's using a look-up table technique. The Figure shows a central processing unit 50 with base and index registers shown generally at 51 and an arithmetic logic unit 52. Associated with the central processing unit 50 is a memory 54. Stored within the memory are state variables shown generally at 55, programs 56 and a series of tables shown at 58. Within the tables 58 are stored the digits of one or more PRBS'S. These digits are stored as groups or words which typically will have, seven or eight digits per group. Groups of digits can be read out from the memory in response to address signals generated by the control processing unit 50.

Data can be fed to the central processing unit via a serial in-parallel out register 60.

In operation when the processor is set to generate a PRBS, an address is generated so that a first group of digits is read from the tables 58. The number of digits or bits within each group is defined by the number of data bits which coccur in a timeslot. This group of bits is also used to determine the address for the next group of bits which is required in the PRBS. In effect what happens is that the state defining value of the PRBS is advanced a number of states per read operation. It will be appreciated that it is not desirable for the software to determine each individual state. What the software does is to identify the next group of digits in a single operation. This is achieved by associating with each given state, the state that will be present after eight clocks. This can be done by the table. The store value in itself used to find the next state and hence the successive states.

The arrangement of Figure 3 shows the base and index registers contained in the CPU 10. It will be appreciated that placement depends upon the associated architectur and it is not necessary for the registers to be in the central processing unit for the algorithm to operate.

Claims

1. Apparatus for monitoring slip in a digital transmission system, in which digital data is received in a store and re-aligned to a local clock, said apparatus being characterised by comprising means (25) for receiving said data from said store and for accumulating a characteristic group of N successive bits of a PRBS sequence transmitted with said data, means (28, 32, 35) for forming groups of N bits of a PRBS sequence which would be expected in the event of a slip, and means (40, 42) for comparing the accumulated N bits with said groups of predicted bits.

2. Apparatus as claimed in claim 1, characterised in that the group of N bits are accumulated from N-n PRBS bits of a first slot (n bits per time slot) and n PRBS bits of the next succeeding time slot.

3. Apparatus as claimed in claim 1 or claim 2, characterised in that the accumulation and generation of expected values is carried out by a processor (20).

4. Apparatus as claimed in claim 3, characterised in that the expected PRBS bits are generated using a look-up table technique.

5. A method for monitoring slip in a digital transmission system in which digital data is received in a store and re-aligned to a local clock, the method being characterised by comprising transmitting a PRBS sequence with said data, accumulating from the received PRBS sequence a characteristic group of N successive bits, forming groups of N bits of a PRBS which would be expected in the event of a slip and comprising the received N bits with the locally formed groups to sense if slip has occurred.

FIG. 1

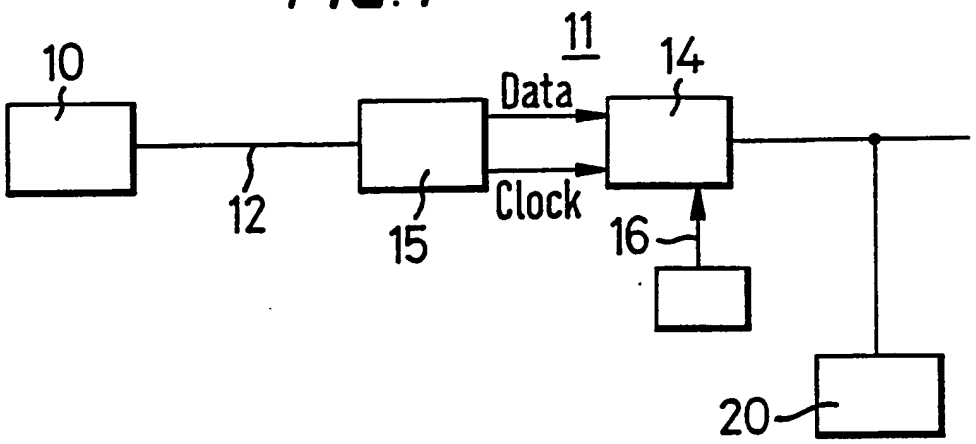

10
11
Data
14
12
15
Clock
16
20

FIG. 2

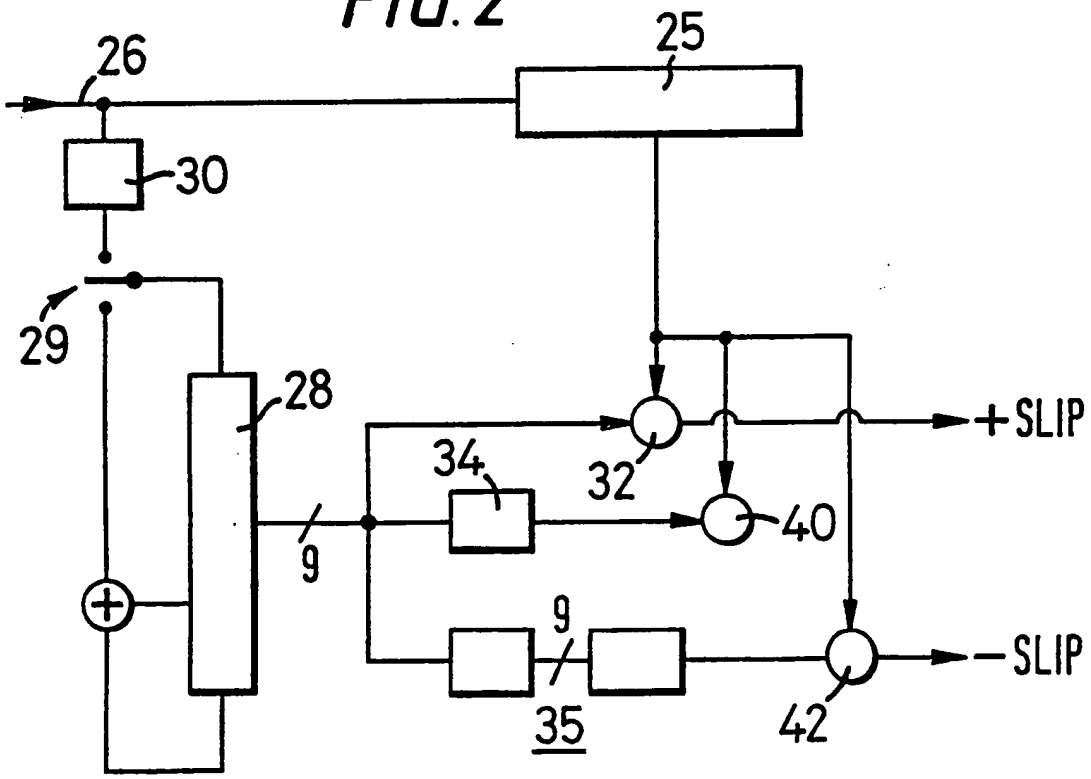
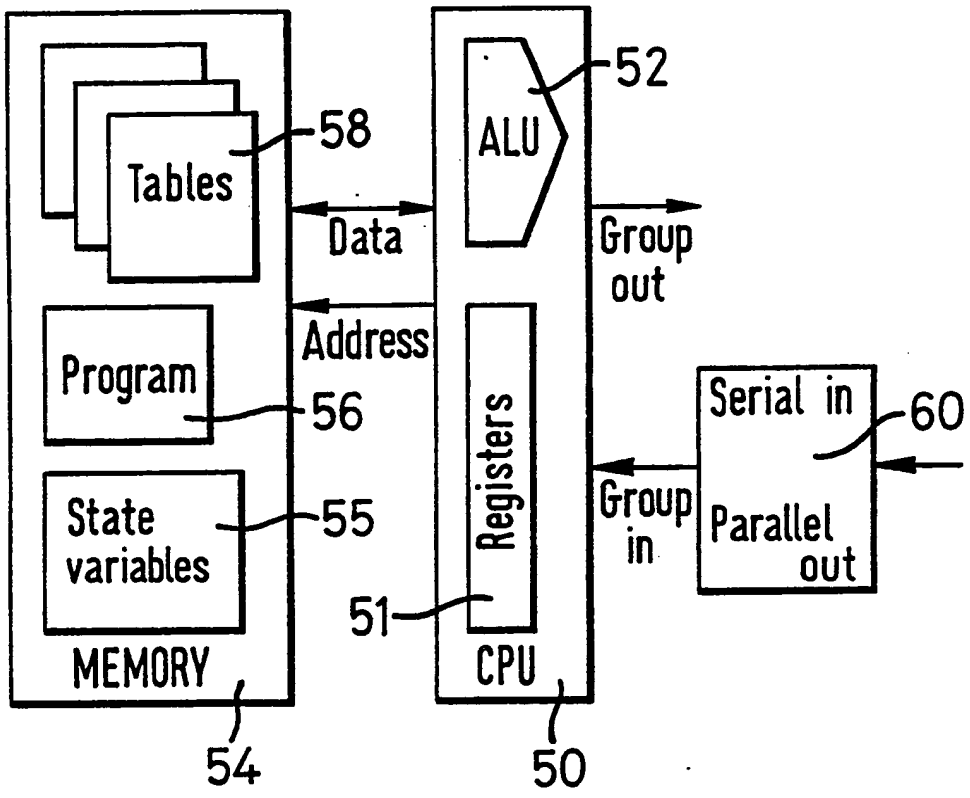

26
25
30
29
28
+SLIP
34
32
40
9
9
-SLIP
35
42

FIG. 3


Tables
58
Program
56
State variables
55
MEMORY
54
Data
Address
ALU
52
Registers
51
CPU
50
Group out
Group in
Serial in
60
Parallel out

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 30 2479

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	HEWLETT-PACKARD JOURNAL, vol. 27, no. 7, March 1976, pages 18-24, Palo Alto, US; I. YOUNG et al.: "A 50-Mbit/s pattern generator and error detector for evaluating digital communications system performance" * Page 9, left-hand column, lines 1-17 *	1-5	H 04 J 3/06
A	EP-A-0 162 658 (AT & T) * Page 1, line 32 - page 2, line 12; page 5, lines 24-28 *	1-5	
A	PATENT ABSTRACTS OF JAPAN, vol. 6, no. 170 (E-128)[1048], 3rd September 1982; & JP-A-57 87 248 (NIPPON DENKI K.K.) 31-05-1982	1-5	
A	DE-B-2 659 512 (WANDEL & GOLTERMANN) * Column 1, line 60 - column 2, line 15 *	4	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 04 J
H 04 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	07-11-1988	VAN DEN BERG,J.G.J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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